Revision History

Rev. No.	History	Issue Date
1.0	Initial issue	Apr.26,2017
2.0	Revise “Chiplus reserves the right to change product or specification without notice” to “Chiplus reserves the right to change product or specification **after approving by customer**.”	Nov. 8, 2021

GENERAL DESCRIPTION

The CS18FS3216W and CS16FS3216W are a 33,578,432-bit high-speed Static Random Access Memory organized as 4M(2M) words by 8(16) bits. The CS18FS3216W (CS16FS3216W) uses 8(16) common input and output lines and have an output enable pin which operates faster than address access time at read cycle, And CS16FS3216W allows that lower and upper byte access by data byte control($\overline{UB}$, $\overline{LB}$).The device is fabricated using advanced CMOS process,6-TR based cell technology and designed for high-speed circuit technology. It is particularly well suited for use in high-density high-speed system applications. The CS18FS3216W and CS16FS3216W are packaged in 48 TFBGA.

FEATURES

- Fast Access Time 10,15ns(Max)
- CMOS Low Power Dissipation
  Standby (TTL) : 70mA (Max.)
  (CMOS) : 55mA (Max.)
  Operating : 120mA (10ns, Max.)
  : 100mA (15ns , Max.)
- Wide range of Power Supply
  - **CSXXFS3216W**: 1.65V~3.6V Power Supply:
- TTL Compatible inputs and Outputs
- Fully Static Operation, No Clock or Refresh required
- Three State Outputs
- Data Byte Control(x16 Mode)
  $\overline{LB}$: I/O$_0$~I/O$_7$, $\overline{UB}$: I/O$_8$~I/O$_{15}$
- Standard 48 TFBGA Package Pin Configurations
- ROHS compliant
- Operating in Commercial and Industrial Temperature range.

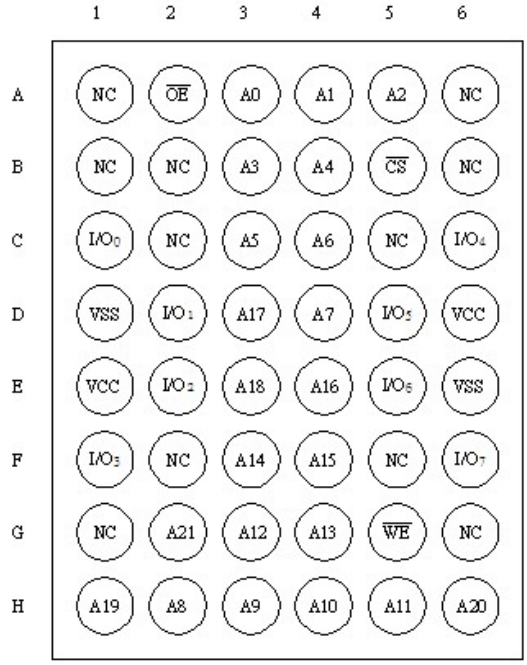
Order Information

Density	Org.	Part Number	V_{CC} (V)	Speed		Package	Temp.
				t_{AA}(ns)	t_{OE}(ns)		
32Mb	4Mx8	**CS18FS3216WHC(I)-10***	2.5~3.3	10	5	48 TFBGA	C : Commercial I : Industrial
			1.8	15	7		
	2Mx16	**CS16FS3216WHC(I)-10***	2.5~3.3	10	5		
			1.8	15	7		

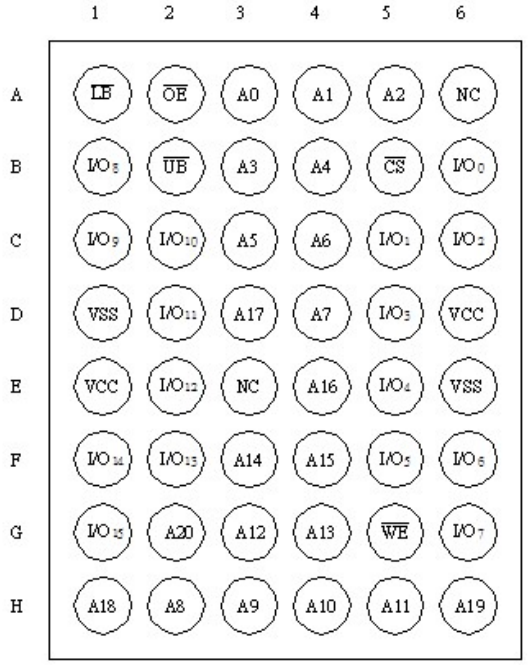
***means max. speed**

PIN CONFIGURATIONS

6x8mm TFBGA with ball pitch 0.75mm

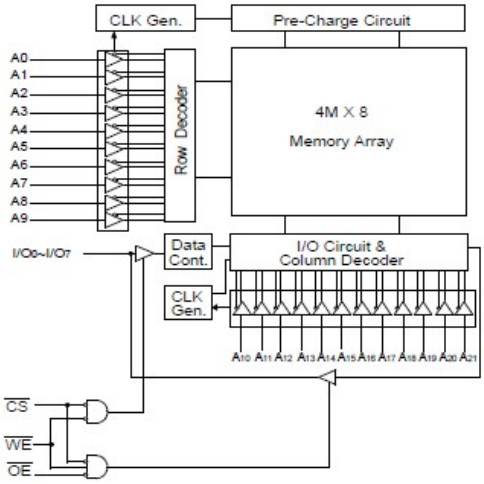


CS18FS3216W – (4M x 8)
Top View

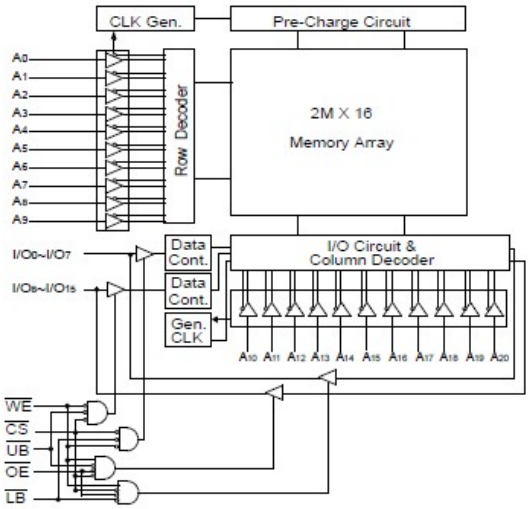


CS16FS3216W – (2M x 16)
Top View

FUNCTIONAL BLOCK DIAGRAM



CS18FS3216W– (4M x 8)



CS16FS3216W – (2M x 16)

Absolute Maximum Ratings*

Parameter		Symbol	Rating	Unit
Voltage on Any Pin Relative to V_{SS}		V_{in}, V_{OUT}	-0.5 to V_{CC}+0.5V	V
Voltage on V_{CC} Supply		V_{in}, V_{OUT}	-0.5 to 4.6	V
Power Dissipation		P_D	1.0	W
Storage Temperature		T_{STG}	-65 to 150	°C
Operating Temperature	Commercial	T_A	0 to 70	°C
	Industrial	T_A	-40 to 85	°C

*Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied.

Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions*(T_A=0 to 70℃)

Parameter	Operating V_{CC}(V)	Symbol	Min.	Typ.	Max.	Unit
Supply Voltage	2.4~3.6	V_{CC}	2.4	2.5/3.3	3.6	V
	1.65~2.2	V_{CC}	1.65	1.8	2.2	
Ground		V_{SS}	0	0	0	V
Input High Voltage	2.4~3.6	V_{IH}	2.0	-	V_{CC}+0.3	V
	1.65~2.2	V_{IH}	1.4	-	V_{CC}+0.2	
Input Low Voltage	2.4~3.6	V_{IL}	-0.3	-	0.7	V
	1.65~2.2	V_{IL}	-0.3	-	0.4	

*The above parameters are also guaranteed for industrial temperature range.

DC and Operating Characteristics*(T_A=0 to 70℃)

Parameter	Symbol	Test Conditions		Min	Max	Unit
Input Leakage Current	I_{LI}	V_{IN}=V_{SS} to V_{CC}		-2	2	uA
Output Leakage Current	I_{LO}	$\overline{CS}$ =V_{IH} or $\overline{OE}$ =V_{IH} or $\overline{WE}$ =V_{IL} V_{OUT}=V_{SS} to V_{CC}		-2	2	uA
Operating Current	I_{CC}	Min.Cycle,100% Duty $\overline{CS}$ =V_{IL}, V_{IN}=V_{IH} or V_{IL},I_{OUT}= 0mA	10ns	-	120	mA
			15ns		100	
Standby Current	I_{SB}	Min. Cycle, $\overline{CS}$ =V_{IH}		-	70	mA
	I_{SB1}	f=0MHz, $\overline{CS}$ ≥V_{CC}-0.2V, V_{IN}≥V_{CC}-0.2V or V_{in}≦0.2V		-	55	
Output Low Voltage Level	V_{OL}	V_{CC} =3.0V, I_{OL}=8mA,(Case of Typical Vcc=3.3V)		-	0.4	V
		V_{CC}=2.4V, I_{OL}=1mA, (Case of Typical Vcc=2.5V)		-	0.4	
		V_{CC}=1.65V, I_{OL}=0.1mA,(Case of Typical Vcc=1.8V)		-	0.2	
Output High	V_{OH}	V_{CC} =3.0V, I_{OH}=4mA,(Case of Typical Vcc=3.3V)		2.4	-	V

Voltage Level		V_{CC} =2.4V, I_{OH}=1mA,(Case of Typical Vcc=2.5V)	2.4	-	
		V_{CC} =1.65V, I_{OL}=0.1mA,(Case of Typical Vcc=1.8V)	1.8	-	

*The above parameters are also guarantee for industrial temperature range.

Capacitance*(T_A= 25℃, f= 1.0MHz)

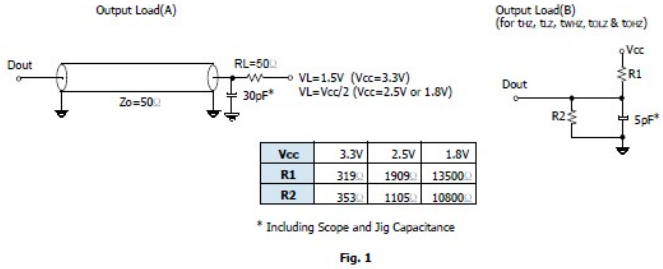
Item	Symbol	Test Conditions	TYP	Max	Unit
Input/ Output Capacitance	$C_{I/O}$	$V_{I/O}$=0V	-	12	pF
Input Capacitance	C_{IN}	V_{IN}=0V	-	10	pF

*Capacitance is sampled and not 100% tested.

Test Conditions*

Parameter	Value
Input/ Output Capacitance	0 to 3.0V (V_{CC}=3.3V)
	0 to 2.5V (V_{CC}=2.5V)
	0 to 1.8V (V_{CC}=1.8V)
Input Rise and Fall Time	1V/1ns
Input and Output Timing Reference Levels	1.5V (V_{CC}=3.3V)
	1/2V_{CC} (V_{CC}= 1.8V or 2.5V)
Output Load	See Fig. 1

*The above parameters are also guaranteed for industrial temperature range.



Vcc	3.3V	2.5V	1.8V
R1	319Ω	1909Ω	13500Ω
R2	353Ω	1105Ω	10800Ω

* Including Scope and Jig Capacitance

Fig. 1

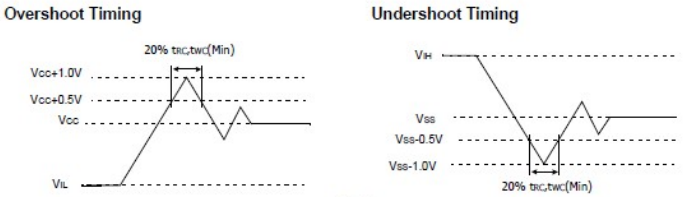


Fig. 2

Functional Description (x8 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	Supply Current
H	X	X*	Not Select	High-Z	I_{SB},I_{SB1}
L	H	H	Output Disable	High-Z	I_{CC}
L	H	L	Read	D_{OUT}	I_{CC}
L	L	X	Write	D_{IN}	I_{CC}

*X means don't care

Functional Description (x16 Mode)

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	$\overline{LB}$ **	$\overline{UB}$ **	Mode	I/O Pin		Supply Current
						I/O_0~I/O_7	I/O_8~I/O_{15}	
H	X	X*	X	X	Not Select	High-Z	High-Z	I_{SB}, I_{SB1}
L	H	H	X	X	Output Disable	High-Z	High-Z	I_{CC}
L	X	X	H	H				
L	H	L	L	H	Read	D_{OUT}	High-Z	I_{CC}
			H	L		High-Z	D_{OUT}	

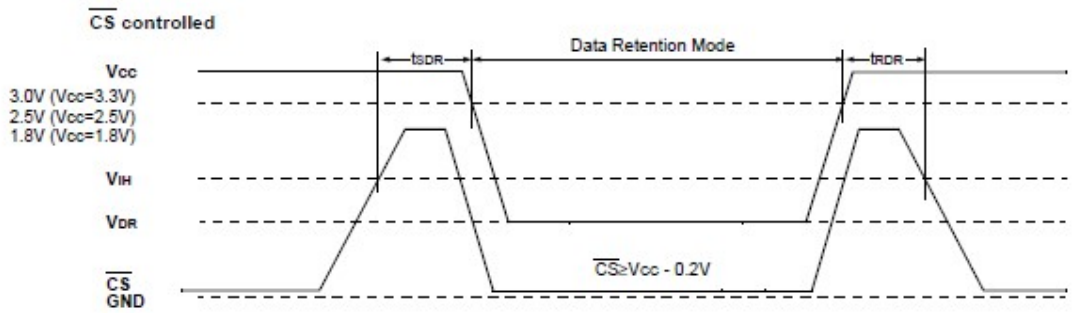
			L	L		D_{OUT}	D_{OUT}	
L	L	X	L	H	Write	D_{IN}	High-Z	I_{CC}
			H	L		High-Z	D_{IN}	
			L	L		D_{IN}	D_{IN}	

*X means don't care

Data Retention Characteristics*(T_A=0 to 70℃)

Parameter	Operating V_{CC}(V)	Symbol	Test Condition	Min.	Typ.	Max.	Unit
V_{CC} for Data Retention	2.4V~3.6V	V_{DR}	$\overline{CS}$ ≥V_{CC} - 0.2V	2.0	-	3.6	V
	1.65V~2.2V			1.5	-	3.6	
Data Retention Current	2.4V~3.6V	I_{DR}	V_{CC}=2.0V $\overline{CS}$ ≥V_{CC} - 0.2V V_{IN}≥ V_{CC} - 0.2V or V_{IN}≤0.2V			55	mA
	1.65V~2.2V		V_{CC}=1.5V $\overline{CS}$ ≥V_{CC} - 0.2V V_{IN}≥ V_{CC} - 0.2V or V_{IN}≤0.2V			55	
Data Retention Set-Up Time		t_{SDR}	See Data Retention Wave form (below)	0			ns
Recovery Time		t_{RDR}		5			ms

Data Retention Wave form



Read Cycle*

Parameter	Symbol	10ns		15ns		Unit
		Min	Max	Min	Max	
Read Cycle Time	t_{RC}	10	-	15	-	ns
Address Access Time	t_{AA}	-	10	-	15-	ns
Chip Select to Output	t_{CO}	-	10	-	15	ns
Output Enable to Valid Output	t_{OE}	-	5	-	7	ns
$\overline{UB}$, $\overline{LB}$ Access Time**	t_{BA}	-	5	-	7	ns
Chip Enable to Low-Z Output	t_{LZ}	3	-	3	-	ns
Output Enable to Low-Z Output	t_{OLZ}	0	-	0	-	ns
$\overline{UB}$, $\overline{LB}$ Enable to Low-Z Output**	t_{BLZ}	0	-	0	-	ns
Chip Disable to High-Z Output	t_{HZ}	0	5	0	7	ns
Output Disable to High-Z Output	t_{OHZ}	0	5	0	7	ns
$\overline{UB}$, $\overline{LB}$ Disable to High-Z Output**	t_{BHZ}	0	5	0	7	ns
Output Hold from Address Change	t_{OH}	3	-	3	-	ns
Chip Selection Power Up Time	t_{PU}	0	-	0	-	ns
Chip Selection Power Down Time	t_{PD}	-	10	-	15	ns

*The above parameters are also guaranteed for industrial temperature range.

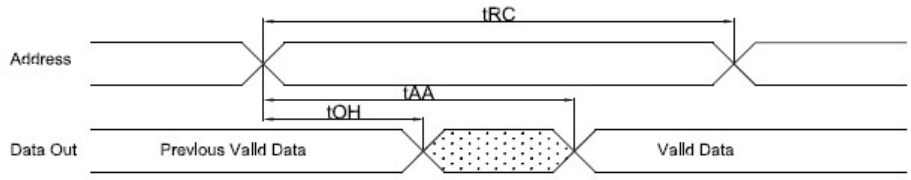
Write Cycle*

Parameter	Symbol	10ns		15ns		Unit
		Min	Max	Min	Max	
Write Cycle Time	t_{WC}	10	-	15	-	ns
Chip Select to End of Write	t_{CW}	7	-	12	-	ns
Address Set-up Time	t_{AS}	0	-	0	-	ns
Address Valid to End of Write	t_{AW}	7	-	12	-	ns
Write Pulse Width($\overline{OE}$ High)	t_{WP}	7	-	12	-	ns
Write Pulse Width($\overline{OE}$ Low)	t_{WP1}	10	-	15	-	ns
$\overline{UB}$, $\overline{LB}$ Valid to End of Write**	t_{BW}	7	-	12	-	ns
Write Recovery Time	t_{WR}	0	-	0	-	ns
Write to Output High-Z	t_{WHZ}	0	5	0	7	ns
Data to Write Time Overlap	t_{DW}	5	-	8	-	ns
Data Hold from Write Time	t_{DH}	0	-	0	-	ns
End of Write to Output Low-Z	t_{OW}	3	-	3	-	ns

*The above parameters are also guaranteed for industrial temperature range.

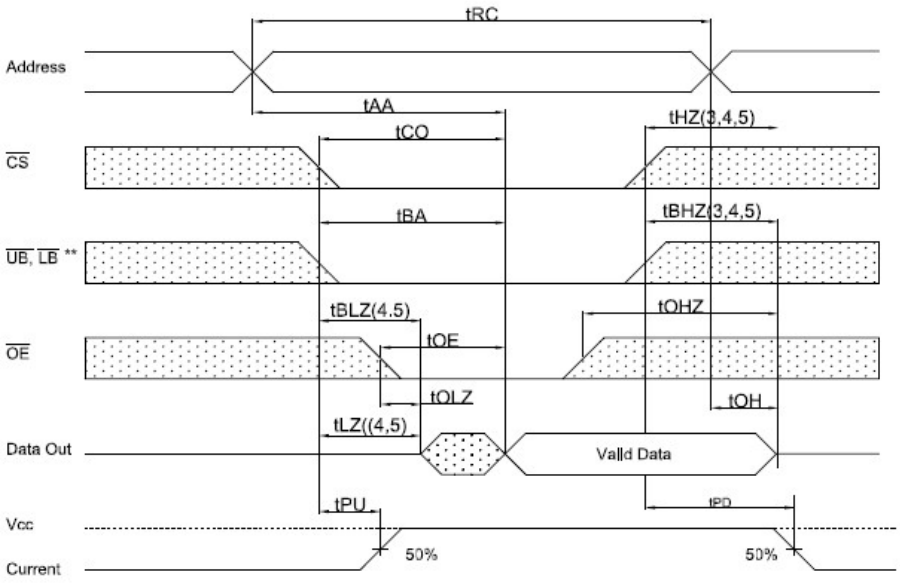
Timing Diagram

Timing Waveform of Read Cycle (1) (Address Controlled, $\overline{CS}$ = $\overline{OE}$ =V_{IL}, $\overline{WE}$ =V_{IH}, $\overline{UB}$, $\overline{LB}$ =V_{IL}**)



**** Those parameters are applied for x16 mode only.**

Timing Waveform of Read Cycle (2) ($\overline{WE}$ =VIH)

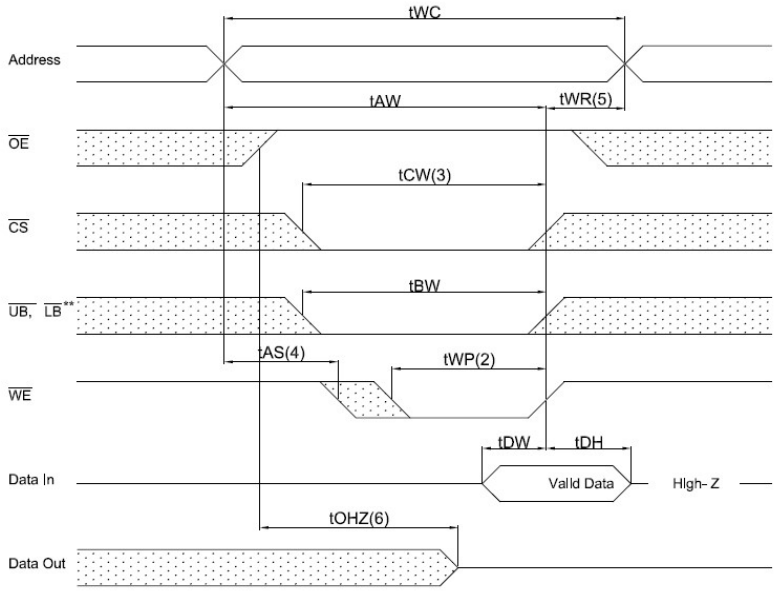


NOTES (Read Cycle)

1. $\overline{WE}$ is high for read cycle
2. All read cycle timing is referenced from the last valid address to the first transition address.
3. t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referenced to V_{OH} or V_{OL} levels.
4. At any given temperature and voltage condition, t_{HZ} (Max.) is less than t_{LZ} (Min.) both for a given device and from device to device.
5. Transition is measured ±200mV from steady state voltage with Load (B). This parameter is sampled and not 100% tested.
6. Device is continuously selected with $\overline{CS}$ =V_{IL}.
7. Address valid prior to coincident with $\overline{CS}$ transition low.
8. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.

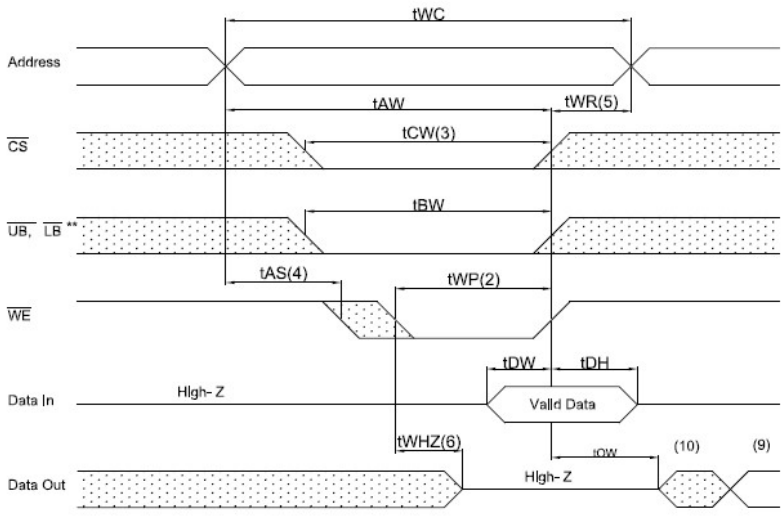
**** Those parameters are applied for x16 mode only.**

Timing Waveform of Write Cycle (1) ($\overline{OE}$ Clock)



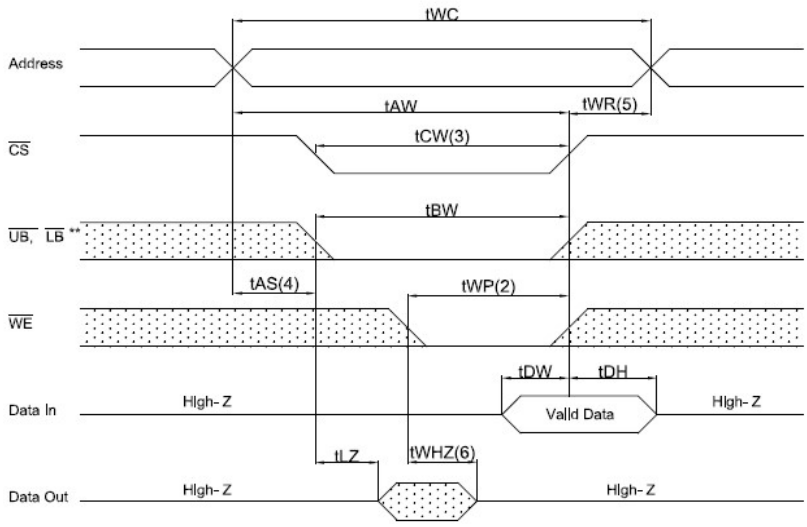
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (2) ($\overline{OE}$ =Low fixed)



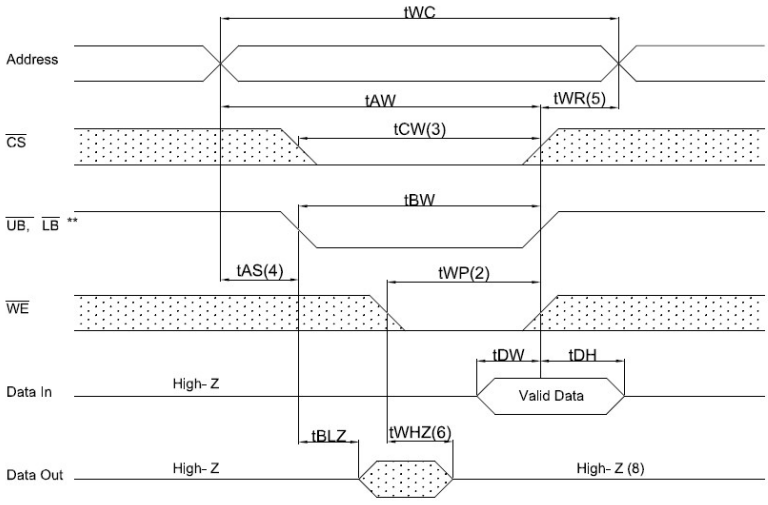
** Those parameters are applied for x16 mode only.

Timing Waveform of Write Cycle (3) ($\overline{CS}$ =Controlled)



**** Those parameters are applied for x16 mode only.**

Timing Waveform of Write Cycle (4) ($\overline{UB}$, $\overline{LB}$ Controlled)



NOTES (Write Cycle)

1. All write cycle timing is referenced from the last valid address to the first transition address.
2. A write occurs during the overlap of a low $\overline{CS}$, $\overline{WE}$, $\overline{LB}$ and $\overline{UB}$. A write begins at the latest transition

$\overline{CS}$ going low and $\overline{WE}$ going low ;

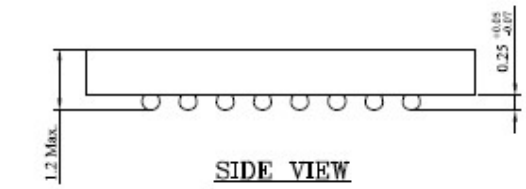
A write ends at the earliest transition $\overline{CS}$ going high or $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

3. t_{CW} is measured from the later of $\overline{CS}$ going low to end of write.
4. t_{AS} is measured from the address valid to the beginning of write.
5. $\overline{WE}$ is measured from the end of write to the address change. t_{WR} applied in case a write ends as $\overline{CS}$ or $\overline{WE}$ going high.
6. If $\overline{OE}$, $\overline{CS}$ and $\overline{WE}$ are in the Read Mode during this period, the I/O pins are in the output low-Z state. Inputs of opposite phase of the output must not be applied because bus contention can occur.
7. For common I/O applications, minimization or elimination of bus contention conditions is necessary during read and write cycle.
8. If $\overline{CS}$ goes low simultaneously with $\overline{WE}$ going or after WE going low, the outputs remain high impedance state.
9. D_{OUT} is the read data of the new address.
10. When $\overline{CS}$ is low : I/O pins are in the output state. The input signals in the opposite phase leading to the output should not be applied.

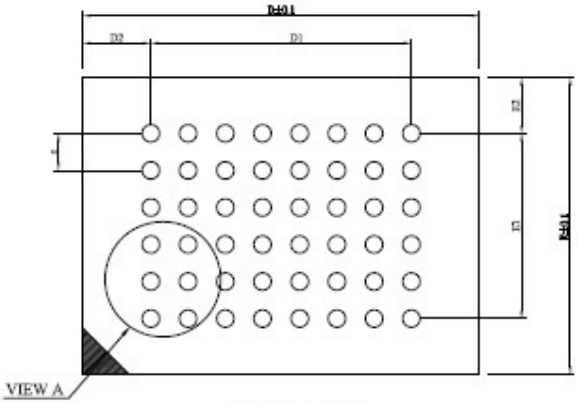
** Those parameters are applied for x16 mode only

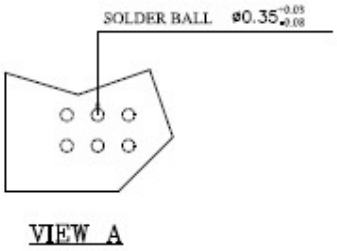
Package outline dimensions

48ball TFBGA-6x8mm (ball pitch: 0.75mm)



BALL PITCH e = 0.75						
D	E	N	D1	E1	D2	E2
8.0	6.0	48	5.25	3.75	1.375	1.125





NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS.
2. PIN#1 DOT MARKING BY LASER OR PAD PRINT.
3. SYMBOL "N" IS THE NUMBER OF SOLDER BALLS.
4. TOLERANCES:
   LINEAR : X.X = ±0.1
   X.XX = ± 0.05
   X.XXX = ± 0.025